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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Raymond J. Beffa

Serial No.: Not yet assigned

Filed: March 6, 2002

For: METHOD FOR SORTING
INTEGRATED CIRCUIT DEVICES

Examiner: Unknown

Group Art Unit: Unknown

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

The present application is a continuation of application Serial No. 09/941,092, filed August 28, 2001, pending, which is a continuation of application Serial No. 09/713,912, filed November 15, 2000, pending, which is a division of application Serial No. 09/520,067, filed March 7, 2000, now U.S. Patent 6,350,959 B1, issued February 26, 2002, which is a continuation of application Serial No. 09/133,338, filed August 13, 1998, now U.S. Patent 6,100,486, issued August 8, 2000, which is a division of application Serial No. 08/785,353, filed January 17, 1997, now U.S. Patent 5,927,512, issued July 27, 1999.

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior applications, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 or PTO/SB/08A form listing all of the information of record in the prior applications is enclosed herewith.

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: March 6, 2002

JRD/sls:djp

Enclosure: Form PTO-1449 or PTO/SB/08A